

ABSTRACT

A multi-channel integrated circuit is provided in which each channel has an analog section and a digital section. Each channel of the readout chip employs low noise charge sensitive amplifier at its input followed by other circuitry such as shaper, pole-zero, peak hold, different comparators, buffers and digital control and readout. Each channel produces a self-trigger and a fast timing output. Channel-to-channel time differences are also recorded. Integrated circuit also provides a large dynamic range to facilitate large range of applications. The trigger threshold can be adjusted to provide energy discrimination. The chip has different, externally selectable, operational modes including a sparse readout mode in which only the channels which have received signals greater than a preselected threshold value are read out. The sparse readout mode results in increased data throughput, thus providing fast data acquisition capabilities.